CLAIMS LISTING

The following listing of claims will replace all prior versions and listings of claims in this application:

1. (Canceled) A PCB with internal signal traces on a thin dielectric layer suspended in air between two flat metal plates. Suspension in air is accomplished by indentation of the flat metal plates above and below the trace and a distance away from the edges of the trace, leaving the remainder of the metal away from the indentation to act as a spacer. The indented area is referred to as a "channel". See FIG. 1 for orthogonal view and FIG. 2 for end-on view.

2. (Canceled) The PCB of claim 1 fabricated by removal of material in the metal plate by etching, milling, punching or shaping or any other method.

3. (Canceled) The PCB of claim 1 fabricated by adding material to the metal plate using buy not limited to plating, welding, electro-plating, painting, spraying, or assembly or any other metal build-up process.

4. (Canceled) The PCB of claim 1 fabricated by assembling a combination of metal plates with at least one plate essentially electrically continuous over the assembly, and at least one metal spacing plate with metal removed from the trace area to keep from shorting the signal. The metal spacing plate(s) may be made by etching, milling punching or any process.

5. (Canceled) The PCB of claim 1 fabricated by shaping of material in the metal plate by but not limited to stamping, drawing or other process. The ridges and valleys of one side can become the valleys and ridges of the opposite side, for the next layer stacked.

6. (Canceled) The PCB of claim 1 fabricated by casting, molding, electro-forming or any similar process to make the metal plate in the desired shape. The ridges and valleys of one side can become the valleys and ridges of the opposite side, for the next layer stacked.

7. (Canceled) The PCB of claim 1 with dielectric layer strong enough to support the trace between the spacing layers but thin enough to minimize the effect it will have on the composite dielectric constant including the air between the trace and the external conductive planes.

8. (Canceled) The PCB of claim 1 wherein several traces may be used on the same dielectric layer in individual channels.

9. (Canceled) The PCB of claim 1 wherein several traces may be placed within a single channel.

10. (Canceled) The PCB of claim 1 wherein two traces may be placed to operate as a differential pair of signals.

11. (Canceled) The PCB of claim 1 wherein Multiple layers are stacked so that many traces can be routed in the same PCB.

12. (Canceled) Single metal plate of claim 1 may have metal indentation on the opposite surface so that the plate serves two different signal traces, one above and one below.

13. (Canceled) The PCB of claim 1 will be 4 or 5 millimeter thick spacers, conductive layers will be about 1 millimeter thick, copper trace will be about 1 millimeter thick and the overall section will be about 12 millimeters.

14. (Canceled) The PCB of claim 1 wherein channels in the metal plates noted above may be extended to the edges of the PCB or to holes to the surface to provide for air escape or inflow if temperature or altitude changes might cause compression or expansion of trapped air and de-lamination.

15. (Canceled) The PCB of claim 1 wherein attachment of vias for traces of claim 1 may be by (1) removing the dielectric layer with signal trace, (2) drilling a hole larger than the via in the metal plates and spacers, (3) forcing dielectric material into the drill hole in the metal plates individually, (4) laminating the layers together, (5) drilling a smaller via hole through the dielectric material and the pads on the signal trance, and (6) plating to connect the via to the signal trace as is normally done.

16. (Canceled) The PCB of claim 1 wherein attachment of vias of claim 1 may be done using several techniques Including the insertion of dielectric spacers or metal pins to electrically connect and to position the connection via.

17. (Canceled) The PCB of claim 1 wherein laminating metal to metal may use an adhesive coating or an adhesive sheet. The adhesive will have no effect on electrical high speed performance because the thin dielectric of the adhesive with wide metal plates forms a high frequency capacitive short from top to bottom plates.

18. (Currently Amended) A multilayered printed circuit board comprising:

a. Three or more layers of conductive material,

i. Including at least one trace layer; and

ii. At least one spacer layer located above the trace layer, and at least one spacer layer located below the trace layer.

b. A dielectric layer with embedded internal signal traces;

i. Wherein the dielectric layer is suspended in air between two metal plates and is separated from the two metal plates by metal spacers;

ii. Wherein the air adjacent to the dielectric layer is allowed to freely flow into and out of the apparatus;

iii. wherein the two metal plates comprise metal spacing elements.

c. At least one via that vertically connects at least two signal traces.

19. (Previously Presented) The printed circuit board of claim 18 further comprising open air channels located in the flat metal plates above and below at least one of the signal traces.

20. (Previously Presented) The printed circuit board of claim 19 wherein the width of open air channels are wider than at least one of the internal signal traces.

21. (Canceled) A method of manufacturing a printed circuit board that contains a plurality of internal signal traces located on a dielectric layer wherein the dielectric layer is suspended in air between two flat metal plates, comprising:

a. A means for creating open air channels in the flat metal plates above and below at least one of the signal traces.

22. (Canceled) The method of manufacturing a printed circuit board of claim 21 wherein the means for creating open air channels in the flat metal plates above and below at least one of the signal traces comprises etching, milling, punching or shaping the open air channels.

23. (Canceled) The method of manufacturing a printed circuit board of claim 21 wherein the means for creating open air channels in the flat metal plates above and below at least one of the signal traces comprises adding material to at least one of the metal plates.

24. (Canceled) The method of manufacturing a printed circuit board of claim 23 wherein the means for adding material to at least one of the metal plates comprises using a metal build-up process, such as plating, welding, electro-plating, painting, spraying, or assembly.

25. (Canceled) The method of manufacturing a printed circuit board of claim 21 comprising:

a. combining a top plate and a top spacer plate such that the top plate and top spacer plate create an open air channel above at least one internal signal trace located on a dielectric layer,

b. wherein the dielectric layer is suspended in air,

c. combining a bottom plate and bottom spacer such that the bottom plate and bottom spacer plate create an open air channel below at least one internal signal trace located on a dielectric layer, and

d. wherein the dielectric layer is suspended in air.

26. (Canceled) The method of manufacturing a printed circuit board of claim 25 wherein the open air channels in the metal spacing plate(s) are made by etching, milling, or punching the metal spacing plate(s).

27. (Previously Presented) The printed circuit board of claim 19 wherein the open air channels in the flat metal plates are located above and below at least one of the signal traces.

28. (Previously Presented) The printed circuit board of claim 19 wherein the open air channels in the flat metal plates allow for air to flow freely through the channel(s).

29. (Previously Presented) The printed circuit board of claim 19 wherein layers on the printed circuit board are laminated together during manufacture.

30. (Previously Presented) The printed circuit board of claim 19 wherein air is used as the primary dielectric in order to pass all high-frequency signals without discrimination.

31. (Previously Presented) The printed circuit board of claim 29 wherein the layers on the printed circuit board are laminated together using an adhesive coating.

32. (New) A laminated air-dielectric multilayer circuit board comprising:

a. top and bottom metal layers spaced from each other, each in parallel planes;

b. an intermediate dielectric layer located intermediate to the top and bottom metal layers;

c. first planer metal spacer layer located between the top metal layer and the intermediate dielectric layer;

d. a second planer metal spacer layer located between the bottom metal layer and the intermediate dielectric layer;

e. each spacer layer having an open air channel formed therein with longitudinally extending solid sidewalls in the spacer defining upper and lower air chambers on opposing faces of the intermediate dielectric layer; and

f. a conductive trace attached to at least one face of the intermediate dielectric layer.

33. (New) The laminated air-dielectric multilayer circuit board of Claim 32, wherein the top planer metal layer and the first metal planer spacer layer is a single metal layer comprising at least one air channel.

34. (New) The laminated air-dielectric multilayer circuit board of Claim 32, wherein the bottom planer metal layer and the second metal planer spacer layer is a single metal layer comprising at least one air channel.

35. (New) The laminated air-dielectric multilayer circuit board of Claim 32, further comprising a plurality of open air channels located in the first and second metal planer spacer layers.

36. (New) The laminated air-dielectric multilayer circuit board of Claim 32, wherein the open air channels allow ambient air to flow into and out of the open air channels.

37. (New) The laminated air-dielectric multilayer circuit board of Claim 32, further comprising vias vertically connecting two or more signal traces.

38. (New) The laminated air-dielectric multilayer circuit board of Claim 32, further comprising vias located between a signal trace and an additional connection point.

39. (New) The PCB of claim 18 further comprising a plurality of internal signal traces located on a dielectric layer, wherein the dielectric layer is suspended in air between two flat metal plates.